UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,063	12/09/2003	Anand Rajagopalan	NVDA P000785	3734

26291 7590 09/28/2009

PATTERSON & SHERIDAN L.L.P. NJ Office
3040 Post Oak Boulevard
Suite 1500
Houston, TX 77056-6582

EXAMINER	
VIDWAN, JASJIT S	
ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
09/28/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Ktaboada@pattersonsheridan.com
psdocketing@pattersonsheridan.com
PAIR_eOfficeAction@pattersonsheridan.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/731,063
Filing Date: December 09, 2003
Appellant(s): RAJAGOPALAN ET AL.

Stephanie Winner
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/11/09 appealing from the Office action mailed 09/04/08

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,334,153	Boucher	12-2001
6629125	Elzur et al.	9-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, & 10, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher et al, U.S. Patent No: 6,334,153 **[hereinafter Boucher]** and further in view of Elzur et al, U.S. Patent No: 6,629,125 **[hereinafter Elzur]**.

1. **As per claims 1**, Boucher teaches a system for uploading frame data to system memory, the system comprising:

(a) CPU coupled to the system memory and configured to execute an application program **[Col. 5, Lines 10-24]**.

(b) CPU executing a Transmission Control Protocol (TCP) stack which includes code to complete at least some TCP processing **[Col. 6, Lines 22-38]**

(c) Hardware subsystem preconfigured to process all frames related to one or more connections delegated by the TCP stack to produce frame data **[Col. 2, Lines 60-67,** *"processing bits of incoming network data"***]** and upload the frame data to a portion of system memory allocated to the application program **[Col. 3, Lines 56-62,** *The Fast-path method delivers data directly to intended destination which is the Application Program***]**

(d) System memory including a connection table (CT) storing data for all active connections with system including delegated connections **[Col. 45, Lines 16-28]**, reads and writes to the CT being made directly through the hardware [Col. 4, Lines 6-10]

(e) Hardware subsystem being further preconfigured to request legacy processing by the TCP stack of the frames of the delegated connections **[Col. 6, Lines 54-56]**

Boucher teaches the above limitation in addition to teaching handling exceptions in conditions where fast path data destined to be transferred directly to user buffer of system memory (35) is rerouted to protocol processing stack (44) and thus to legacy buffer due to any given exceptions that might arise **[see Col. 5, Lines 55-Col. 6, Lines 5]**. Boucher, however, does not disclose transferring data to a legacy

buffer in portion of system shared memory not allocated to application program and further transferring the data from the legacy buffer to application program prior to use. Elzur of analogous art teaches the above teaching of storing the data directly in application memory **[see Elzur, Fig. 7, element 304]** and storing incoming data in memory not designated for application when application buffer is not available **[see Elzur, Fig. 7, element 308]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above to two teachings in order to take advantage of preventing error through either overflow or when the data is transmitted out of order. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings.

2. **As per Claim 10**, Boucher as modified by Elzur above teaches a method of uploading frame data including Transmission Control Protocol (TCP) payload data **[Col. 6, Lines 22-38]** to system memory, the method comprising

(a) Processing a frame to produce frame data **[Col. 2, Lines 60-67,** *"processing bits of incoming network data"***]**

(b) Uploading the frame data to either a portion of system memory comprising a user buffer allocated to an application program **[Col. 3, Lines 56-62,** *The Fast-path method delivers data directly to intended destination which is the Application Program***]** or a legacy buffer in the system memory for separate TCP processing by a TCP stack executing on a CPU depending on whether the user buffer is available **[Col. 2, Lines 44-59,** *The slow-path method adds headers of each layer prior to sending the frame to the second host***]**

(c) Copying frame data uploaded to legacy buffer from the portion of the system memory not allocated to the application memory to the system memory that is allocated to application memory **[see Elzur, Col. 5, Lines 29-44 – When the data is not transmitted to the application memory (304), the data is placed temporarily in space not allocated to application memory (308) prior to being moved to 304. Elzur gives an example of a scenario wherein the data packet/frame arrives at the network node out of order. Therefore, rather than placing the**

said packet in the application buffer and thereby generating an error, the data packet is placed in shared memory 308 prior to being moved to 304 after the missing packets arrive].

(d) Utilizing hardware separate from the CPU which does the TCP processing**]** to partially process the frame and determine whether the frame was delegated by the separate TCP processing **[Col. 4, Lines 6-10,** *"The specialized microprocessor and the host intelligently choose whether a given message or portion of a message (partially processed frame) is processed by the microprocessor (hardware) or the host stock (software)"***]**

3. **As per claims 2**, Boucher as modified by Elzur above teaches a system wherein the frame data is payload data **[Col. 2, Lines 60-67,** *data without headers***]**

4. **As per claims 3**, Boucher as modified by Elzur above teaches a system wherein a TCP Stack **[Col. 6, Lines 22-38**, data handled by TCP protocols, therefore TCP stack handles fast-path data**]** provides the hardware with a physical address corresponding to a user buffer **[Col. 18, Lines 61-63]**

5. As per Claims 29 & 30, Boucher as modified by Elzur above teaches a system wherein the portion of system memory that stores the legacy buffer is allocated to a software driver **[see Chmielecki, Col. 17, Lines 56-59]**.

6. Claims 4-6, 8-9,21-22, 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher & Elzur and further in view of Adams, U.S. Patent No: 6,775,693 **[herein after Adams]**.

7. **As per claims 4, 5 and 6**, Boucher as modified by Elzur above teaches the limitations of claims 1 and 10. Boucher further teaches a method for slow-path processing which is the conventional method of transferring and processing data where the frame data is moved to a secondary storage prior to being processed by the Host. However, Boucher does not explicitly teach system wherein the hardware is configured to process frames to produce partially processed frame data and further uploading the partially processed frame data to a portion of system memory allocated to a software driver. However, Adams teaches a system wherein the hardware is configured to process frames to produce partially processed

frame data and further uploading the partially processed frame data to a portion of system memory allocated to a software driver **[See Adams, Col. 8, Lines 38-45]**.

It would have been obvious for one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Boucher with that of Adams in order to take advantage of having a dual option for the microprocessor and the host to intelligently choose whether a given message or portion of a message is processed by fast-path or slow-path **[Col. 4, Lines 5-10]**. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings in order to take advantage of having a dual option for the microprocessor and the host to intelligently choose whether a given message or portion of a message is processed by fast-path or slow-path **[Col. 4, Lines 5-10]**.

8. **As per claims 8**, teachings of Boucher & Elzur as modified by Adams teach a system wherein a software driver provides the hardware with a tag corresponding to a location of the legacy buffer **[See Adams, Col. 8, Lines 46-51]**

9. **As per claim 9**, teachings of Boucher & Elzur as modified by Adams teach a system wherein the hardware is configured to transmit the tag to the software driver **[See Adams, Col. 8, Lines 38-45].**

10. **As per Claim 21,** teachings of Boucher & Elzur as modified by Adams teach a system wherein the hardware is configured to pause incoming frame data to determine whether a frame is invalid, the invalid frame being stored in the legacy buffer for legacy processing **[Col. 58, Lines 9-29]**.

11. **As per Claim 22,** teachings of Boucher & Elzur as modified by Adams teach a system wherein the TCP stack is configured to process the frame data up loaded to the legacy buffer by the hardware **[Col. 2, Lines 44-59]**

12. **As per Claim 24,** teachings of Boucher & Elzur as modified by Adams teach a method wherein the TCP stack completes processing of the partially processed frame stored in the legacy buffer **[Fig. 4, element 62, "Cache"]**.

13. **As per Claim 25,** teachings of Boucher & Elzur as modified by Adams teaches a method wherein the partial processing of the frame produces partially processed frame and header data **[See Adams, Col. 8, Lines 38-45]**

14. **As per Claim 26**, teachings of Boucher & Elzur as modified by Adams teach a method wherein the user buffer is defined as not available when the processed frame portion exceeds a start up limit value associated with the delegated connection carrying the frame being processed **[Col. 2, Lines 60 – Col. 3, Line 5]**

15. **As per Claim 27**, teachings of Boucher as Elzur by Adams teach a method wherein the uploaded frame data includes TCP payload data **[Col. 6, Lines 22-38]**

16. **As per Claim 28,** teachings of Boucher as Elzur by Adams teach a system wherein the hardware accesses the CT using the distribution port field of a frame as a direct index into the CT **[Col. 6, Line 66 - Col. 7, Line 15]**

(10) Response to Argument

Appellant's Argument: Prior art fails to teach or suggest that frame data is uploaded to a legacy buffer in a portion of the system memory that is not allocated to the application program if a user buffer is not available. Specifically, Appellant argues that the secondary reference (Elzur) teaches portion of memory designated to application program and separate portion not designated to application program are part of the same buffer and thus there is no distinction between "legacy buffer" and "user buffer."

Examiner's response: It is true that the secondary reference teaches just one memory structure (Fig. 7, element 304) divided into "application portion" (Fig. 7, element 306) and "non-application portion" (Fig. 7, element 308). Data is stored in the application portion unless there is a condition such as out of sequence packet in which case, the incoming data will be stored to "non-application" portion and then later moved to the "application portion" of the memory.

Applicant's argument that prior art does not teach two "distinct" buffers (since 306 & 308 are both part of memory 304) is improper in view of Examiner because a "buffer" is defined by Microsoft Computer Dictionary (Fifth Edition) as "region of memory reserved for use as an intermediate repository in which data is temporarily held..." Therefore, holding true to that definition, it would be obvious to one of ordinary

skill in the art that a single memory structure having separate applicable reserved regions therein for "user buffer" - (Fig. 7, element 306) & "legacy buffer" - (Fig. 7, element 308) would read on the claimed invention as taught by Elzur. Furthermore, it should be noted that though the memory structure (element 304) is designated as "Application layer" - only the packets received in memory region 306 are processed by the Application in question whereas the memory region 308 is used as temporary storage for control issues (See Col. 5, Lines 37-44) which then requires the said packets to be moved to the application portion of the memory (306) from the shared memory (308) after the said issue has been resolved.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jasjit Vidwan/

Patent Examiner Art unit: 2182

Conferees:

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117

/Tariq R. Hafiz/
Supervisory Patent Examiner (2182)